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EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/719,523	ISONO ET AL.	
	Examiner	Art Unit	
	Prabodh M Dharia	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-53* is/are pending in the application.

4a) Of the above claim(s) *1-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-44 and 47-53* is/are rejected.

7)☒ Claim(s) *45 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04-22-2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. **Status:** Receipt is acknowledged of papers submitted on 07-16-2004 under amendments and new claims have been placed of record in the file. Claims 34-53 are pending in this action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 34-44,48-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Takegami et al. (6,288,485 B1).

Regarding Claim 34, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons from an electron source (Col. 7, Lines 4-6, Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); a pulse generating circuit for generating pulse signals at a predetermined time period (Col. 18, Lines 11-30, each horizontal sync the control circuit lights up each individual pixel through a switch that supplies the data for the pixel, since each horizontal scan is has fixed number of pixels the control circuit generate predetermined number of pulses per data for the

pixels Col. 17, Lines 38-44, Lines 47-62, Col. 17, Line 63 to Col. 18, line 10); and a control circuit for stopping output from the scanning circuit and/or the modulation circuit to the display panel until said pulse generating circuit generates a predetermined number of pulse signals pulse (Col. 18, Lines 11-30, each horizontal sync the control circuit lights up each individual pixel through a switch that supplies the data for the pixel, since each horizontal scan a fixed pre determined time period, and has fixed number of pixels the control circuit generate predetermined number of pulses per data for the pixels Col. 17, Lines 38-44, Lines 47-62, Col. 17, Line 63 to Col. 18, line 10); at the initial stage after a power source is turned on (Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed.).

Regarding Claim 35, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons from an electron source (Col. 7, Lines 4-6, Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); a pulse generating circuit for generating pulse signals at a predetermined time period (Col. 18, Lines 11-30, each horizontal sync the control circuit lights up each individual pixel through a switch that supplies the data for the pixel, since each horizontal scan is has fixed

number of pixels the control circuit generate predetermined number of pulses per data for the pixels Col. 17, Lines 38-44, Lines 47-62, Col. 17, Line 63 to Col. 18, Line 10, Col. 18, Lines 47-52); and a control circuit for controlling said scanning circuit and/or said modulation circuit so as to output the scanning signal and/or the modulation signal (Col. 18, Lines 47-52) after said pulse generating circuit generates a predetermined number of pulse signals at the initial stage after a power source is turned on (Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed.).

Regarding Claim 36, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to said display panel an acceleration potential for accelerating electrons (Col. 7, Lines 4,5, Col. 4, Lines 21-42, figure 9A, 9B, Col. 15, Lines 22-28) from an electron source; a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a control circuit for stopping output from the scanning circuit and/or the modulation circuit to the display panel until a signal output from the scanning circuit and/or the modulation circuit to the display panel is determined at the initial stage after a power source is turned on (Col. 9, Lines 31-42, Col. 14, Line 62 to Col.

15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed.).

Regarding Claim 37, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a control circuit for delaying output of a signal from the scanning circuit and/or the modulation circuit to the display panel at the initial stage after a power source is turned on (Col. 14, Lines 62-65) in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel, wherein the signal output from the scanning circuit and/or the modulation circuit to the display panel is determined during the delay time (Col. 16, Line 50 to Col. 17, Line 14, Col. 17, Lines 38-44, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan, however, during the retrace time signal to pane is delayed from control circuit and also from scan circuit and modulation circuit Col. 18, Lines 11-53).

Regarding Claim 38, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a control circuit for stopping output from the scanning circuit and/or the modulation circuit to the display panel until a power source voltage of the scanning circuit and/or the modulation circuit reaches a desired value at the initial stage after a power source is turned on (Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed, Col. 16, Line 50 to Col. 17, Line 14, Col. 17, Lines 38-44, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan Col. 18, Lines 11-53).

Regarding Claim 39, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, 35-44); a modulation circuit for supplying a modulation signal to the display panel

(Col. 18, Lines 47-52); and a control circuit for delaying output of a signal from the scanning circuit and/or the modulation circuit to the display panel at the initial stage after a power source is turned on (Col. 14, line 62-65) in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel, wherein a power source voltage of the scanning circuit and/or the modulation circuit reaches a desired value during the delay time (Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed, Col. 16, Line 50 to Col. 17, Line 14, Col. 17, Lines 38-44, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan Col. 18, Lines 11-53).

Regarding Claim 40, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source (Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a control circuit for stopping supply of the acceleration potential until a power source

voltage of the scanning circuit and/or the modulation circuit reaches a desired value at the initial stage after a power source is turned on (Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed, Col. 16, Line 50 to Col. 17, Line 14, Col. 17, Lines 38-44, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan Col. 18, Lines 11-53).

Regarding Claim 41, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source (Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a control circuit for delaying supply of the acceleration potential at the initial stage after a power source is turned on in starting image display by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel, wherein a power source voltage of the scanning circuit and/or the modulation circuit reaches a desired value during the

delay time (Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed, Col. 16, Line 50 to Col. 17, Line 14, Col. 17, Lines 38-44, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan, however, during the retrace time signal to pane is delayed from control circuit and also from scan circuit and modulation circuit Col. 18, Lines 11-53).

Regarding Claim 42, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source (Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); a control circuit for stopping output of a signal from the scanning circuit and/or the modulation circuit to the display panel, and then stopping supply of power to the scanning circuit and/or the modulation circuit In turning off a power source while an image is displayed by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel.

Regarding Claim 43, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source (Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a control circuit for stopping output of a signal from the scanning circuit and/or the modulation circuit to the display panel, and then stopping supply of power to the scanning circuit and/or the modulation circuit in performing emergency shutdown (Col. 15, Lines 13-28) while an image is displayed by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel (Col. 16, Line 50 to Col. 17, Line 14, Col. 17, Lines 38-44, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan Col. 18, Lines 11-53).

Regarding Claim 44, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source (Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-

44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a control circuit for stopping output of a signal from the scanning circuit and/or the modulation circuit to the display panel, and then stopping supply of power to the scanning circuit and/or the modulation circuit when a voltage abnormality (Col. 15, Lines 22-28) is observed while an image is displayed by outputting a signal from the scanning circuit and/or the modulation circuit to the display panel (Col. 16, Line 50 to Col. 17, Line 14, Col. 17, Lines 38-44, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan Col. 18, Lines 11-53).

Regarding Claim 48, Takegami et al. teaches the electron source comprises a plurality of row-direction wiring lines for receiving a scanning signal, a plurality of column-direction wiring lines for receiving a modulation signal, and a plurality of electron-emitting devices connected to the row-direction wiring lines and the column-direction wiring lines (Col. 3, Lines 52-67, Col. 17, Line to Col. 18, Line 10).

Regarding Claim 49, Takegami et al. teaches the acceleration potential for accelerating electrons from the electron source is a potential higher by not less than 500 V than a potential applied to emit electrons in the electron source (Col. 4, Lines 21-31, Several hundred volts, 100-900V).

Regarding Claim 50, Takegami et al. teaches the acceleration potential for accelerating electrons from the electron source is a potential higher by not less than 3,000 V than a potential applied to emit electrons in the electron source (Col. 4, Lines 21-31, Several kV, 1kV-999kV).

Regarding Claim 51, Takegami et al. teaches the acceleration potential for accelerating electrons from the electron source is a potential higher by not less than 5,000 V than a potential applied to emit electrons in the electron source (Col. 17, Lines 53-62).

Regarding Claim 52, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to said display panel an acceleration potential for accelerating electrons (Col. 7, Lines 4,5, Col. 4, Lines 21-42, figure 9A, 9B, Col. 15, Lines 22-28) from an electron source; a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a pulse generating circuit for generating pulse signals at predetermined time period (Col. 18, Lines 11-30, each horizontal sync the control circuit lights up each individual pixel through a switch that supplies the data for the pixel, since each horizontal scan is has fixed number of pixels the control circuit generate predetermined number of pulses per data for the pixels Col. 17, Lines 38-44, Lines 47-62, Col. 17, Line 63 to Col. 18, Line 10, Col. 18, Lines 47-52); and a control circuit for stopping supply of the acceleration potential (Col. 4, Lines 21-42) until said pulse generating circuit outputs a

predetermined number of pulse signals at the initial stage after a power source is turned on (Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed, Col. 18, Lines 11-30, each horizontal sync the control circuit lights up each individual pixel through a switch that supplies the data for the pixel, since each horizontal scan a fixed pre determined time period, and has fixed number of pixels the control circuit generate predetermined number of pulses per data for the pixels Col. 17, Lines 38-44, Lines 47-62, Col. 17, Line 63 to Col. 18, Line 10, Col. 16, Line 50 to Col. 17, Line 14, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan Col. 18, Lines 11-53).

Regarding Claim 53, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to said display panel an acceleration potential for accelerating electrons (Col. 7, Lines 4,5, Col. 4, Lines 21-42, figure 9A, 9B, Col. 15, Lines 22-28) from an electron source; a scanning circuit for supplying a scanning signal to the display panel (Col. 17, Lines 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a pulse generating circuit for

generating pulse signals at predetermined time period (Col. 18, Lines 11-30, each horizontal sync the control circuit lights up each individual pixel through a switch that supplies the data for the pixel, since each horizontal scan is has fixed number of pixels the control circuit generate predetermined number of pulses per data for the pixels Col. 17, Lines 38-44, Lines 47-62, Col. 17, Line 63 to Col. 18, Line 10, Col. 18, Lines 47-52); and a control circuit for controlling said acceleration potential supply circuit so as to supply the acceleration potential (Col. 4, Lines 21-42) after said pulse generating circuit outputs a predetermined number of pulse signals at the initial stage after a power source is turned on (Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed, Col. 18, Lines 11-30, each horizontal sync the control circuit lights up each individual pixel through a switch that supplies the data for the pixel, since each horizontal scan a fixed pre determined time period, and has fixed number of pixels the control circuit generate predetermined number of pulses per data for the pixels Col. 17, Lines 38-44, Lines 47-62, Col. 17, Line 63 to Col. 18, Line 10, Col. 16, Line 50 to Col. 17, Line 14, Col. 15, Lines 22-28, Control circuit detect of the vertical Sync and starts scanning and detects horizontal scan starts data modulation to display panel and stops modulation of data at the end of horizontal scan and stops scanning at the end of vertical scan Col. 18, Lines 11-53).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takegami et al. (6,288,485) in view of Stendardo et al. (6,064,125) and Kataoka et al. (5,751925).

Regarding Claim 45, Takegami et al. teaches an image display apparatus (Col. 3, Lines 23-31) comprising: a display panel (Col. 3, Lines 28-31) for displaying an image by irradiation a fluorescent substance with electrons (Col. 7, Lines 4,5) from an electron source to (Col. 7, Lines 4-6, Col. 4, Lines 32-42); an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source (Col. 4, Lines 32-42); a scanning circuit for supplying a scanning signal to the display panel (Col. 17, 35-44); a modulation circuit for supplying a modulation signal to the display panel (Col. 18, Lines 47-52); and a first power source for supplying power to the acceleration potential supply circuit and/or the scanning circuit and/or the modulation circuit (Col. 17, Line 47 to Col. 18, Line 52).

However, Takegami et al. fails to teach a second power source for supplying power.

However, Stendardo et al. teaches a second power source for supplying power (Backup power supply (Col. 1, Lines 52-67).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching of Stendardo et al. in Takegami et al. teaching for having an uninterruptible power supply unit in a self–contained housing for coupling between an adapter and an electronic device with polarity sensing system and a polarity switch.

Takegami et al. teaches a first power source for supplying power to the acceleration potential supply circuit and/or the scanning circuit and/or the modulation circuit (Col. 17, Line 47 to Col. 18, Line 52).

However, Takegami et al. fails to teach a control circuit to stop using the power for video at the initial stage after switching from said first power source to said second power stage.

However, Kataoka et al. teaches a control circuit to stop using the power for video at the initial stage after switching from said first power source to said second power stage (Col. 3, Lines 46-67, Col. 4, lines 14-35 Col. 6, Lines 11-17, Lines 33-41, Col. 9, Lines 10-67).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching of Kataoka et al. in Takegami et al. teaching for having an uninterruptible power supply unit and reduce power consumption.

Allowable Subject Matter

6. Claims 46,47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

an image display apparatus comprising: a display panel for displaying an image by irradiation a fluorescent substance with electrons from an electron source to; an acceleration potential supply circuit for supplying to the display panel an acceleration potential for accelerating electrons from the electron source; a scanning circuit for supplying a scanning signal to the display panel; a modulation circuit for supplying a modulation signal to the display panel; a pulse generating circuit for generating pulse signals at a predetermined time period; and **a control circuit for stopping output from the scanning circuit and/or the modulation circuit to the display panel until said pulse generating circuit generates a predetermined number of pulse signals pulse; at the initial stage after a power source is turned on and a first power source for supplying power to the acceleration potential supply circuit and/or the scanning circuit and/or the modulation circuit and a second power source for supplying power to said scanning circuit and/or said modulation circuit upon an abnormal state and a control circuit for stopping output from said supply of the acceleration potential to the scanning circuit and/or the modulation circuit at the initial stage after switching from said first to said second power source, wherein abnormal state is emergency shutdown and second power source comprises a capacitor or a battery.**

The cited references on 892's fail to anticipate or recite individually as well as render obviousness individually and in combination above bold and underlined.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

8. Applicant's arguments filed July 16, 2004 have been fully considered but they are not persuasive.

Applicant argues the cited reference Takegami et al. fails to teach per amended claims pulse generating circuit outputs a predetermined number of pulse signals at the initial stage after a power source is turned on.

Examiner disagrees as Takegami et al. does teach per amended claims pulse generating circuit outputs a predetermined number of pulse signals at the initial stage after a power source is turned on Col. 9, Lines 31-42, Col. 14, Line 62 to Col. 15, Line 28 the timing required from off power supply to saturation is per fabrication of device is being predetermined timing so that size and power requirement of the device meets specification requirement, so the number of pulses required will be predetermined as they are turned off as the saturation is achieved and activation or initial stage is completed, and video process is delayed or does not get started until initial stage is completed).

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is informed that all of the other additional cited references either anticipate

or render the claims obvious. In order to not to be repetitive and exhaustive, the examiner did draft additional rejection based on those references.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamanobe et al. (JP 07-235255 Electron emission element and its manufacture, and electron source using that electron emission element, and image formation device.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231. The examiner can normally be reached on M-F 8AM to 5PM.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

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October 07, 2004

VIJAY SHANKAR
PRIMARY EXAMINER